

Tm Field-free Deterministic Switching of perpendicularly magnetized ferrimagnet in TmIG/ WTe₂ heterostructure

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Abstract

Field free deterministic switching of the magnetization state of a magnet with an out-of-plane magnetic moment by spin-orbit torque is the essential to energy efficient data storage devices. This requires an out-of-plane spin polarization which can be generated in low-crystal symmetry quantum materials. Here we broaden the previous demonstration of spin orbit torque magnetic switching with ferromagnetic Fe₃GeTe₂ (FGT) and Tungsten ditelluride (WTe₂) heterostructure to a ferrimagnetic insulator, Thulium iron garnet (TmIG) and WTe₂ heterostructure.

I. Background

In the previous demonstration of spin orbit torque magnetic switching in Tungsten ditelluride (WTe₂) and Fe₃GeTe₂ (FGT) heterostructures, a charge current flowing in WTe₂ induces a spin polarization with an out of plane component at the interface between WTe₂ and FGT due to its broken in-plane symmetry. This current is used to control the magnetization of FGT and show that deterministic switching can be achieved¹. This type of deterministic switching has applications in energy efficient data storage devices. FGT has an out-of-plane magnetic moment which is preferred in the data storage applications due to the improved stability in high density devices, compared to the in-plane magnetized materials. The magnetization state of FGT is detected by measuring the Anomalous Hall resistance induced by the out-of-plane magnetization of FGT².

In this experiment instead of using the ferromagnetic FGT we used Thulium iron garnet (TmIG), an insulating ferrimagnet. Ferrimagnetic materials have antiparallel spins on neighboring atoms, but the moments do not cancel and so there is a net magnetic moment. As the ferrimagnet has a smaller magnetic moment, the switching is more efficient since it needs a smaller amount of current to switch and the Gilbert damping in the material is smaller^{5,6}, therefore we expect to see faster deterministic switching. TmIG has the same out of plane magnetic moment as FGT which makes it an ideal material to study. The ferrimagnetic phase persists at room temperature so it may be usable in higher temperature applications. TmIG is an insulator, thus all the current flows in WTe₂, meaning that switching is clearer since all the current flows in WTe₂. There is no shunting, and the spin polarization can only be caused by charge current flowing in WTe₂.

We measure the deterministic switching electrically using the voltage difference that occurs from the proximity induced anomalous Hall Effect, as in the previous experiment. To begin, recall the ordinary Hall effect where current flows through a conductor in a perpendicular magnetic field. As the magnetic field exerts a force moving the charge carriers (in this case, the electrons) to one side of the conductor, a voltage difference linearly proportional to the magnetic field can be measured. The anomalous Hall effect³ is observed in ferromagnetic materials. Electrons with opposite spin carrying opposite quantized Hall conductance can be switched, and this leads to a large voltage drop proportional to the out-of-plane magnetization compared to the ordinary Hall effect⁴.

In recent study of TmIG/ Pt bilayer⁷, the Pt atoms at the interface between Pt and TmIG can be magnetized by TmIG due the proximity effect which would allow electric detection of the magnetization state of TmIG. This proximity effect may also occur at the interface of TmIG and WTe₂ and can therefore be used to detect the magnetization of TmIG. If the proximity effect is absent or negligible, then the next

step would be to use Magnetic optical Kerr effect (MOKE). In MOKE linearly or circularly polarized lasers are shone on the sample. This allows for the magnetization direction to reflect in a specific way and will allow for a map of the magnetization in domains and can be used to optically detect switching.

II. Methods

The WTe_2 is an air sensitive material so the fabrication process needs to prevent WTe_2 being exposed to air. In the previous experiment, the WTe_2 and FGT flakes are stacked on the pre-written electrodes and capped by hexagonal boron nitride (hBN) to ensure the interface is clean and the flakes are intact. Unlike FGT, TmIG is grown on Substituted Gadolinium Gallium Garnet (SGGG), a substrate, and cannot be transferred like 2D materials. To ensure the quality of the interface between TmIG and WTe_2 , WTe_2 needs to be stacked on the TmIG before the electrodes can be made. To prevent exposure to air after the stack, WTe_2 is capped by the insulating hBN. This means that an electric contact needs to be made through exposing the side of the WTe_2 .

The usual method of device fabrication is to write the electrodes for electric contact and then stack onto the electrodes. However, the TmIG material cannot be picked up with the usual method since it is grown and so for this experiment a side contact device must be used. Therefore, the first step in this experiment is to test out a side contact device for the WTe_2 and hBN. We have made a side contact device with WTe_2 . The process of making this sample is explained below. The side surface will be oxidized but the oxidized surface will be cleaned by argon sputtering prior to the deposition of metal.

Process from Exfoliation to Mounting (side contact device):

Here I will outline the process from exfoliation to mounting that goes into making the WTe_2 side contact device. The process of exfoliation starts with dicing silicon chips. The silicon chips used have 300 nm of SiO_2 on top where the flakes will be placed. Using a diamond scribe and a glass slide the SiO_2 wafers are cut into square chips and cleaned by sonication in Acetone for 10 minutes and for 5 minutes in Isopropyl alcohol (IPA). This ensures that the chips are clean, and the flakes will stick to them. The actual exfoliation starts with WTe_2 exfoliated in an argon environment in a glove box in which the water and oxygen levels are controlled under 0.01 ppm. WTe_2 is exfoliated using the typical tape method. Taking a few flakes of WTe_2 it is placed onto one side of a sticky tape. Then using the other strip of sticky tape, the flakes of bulk are slowly made thinner and spread out from the initial place that they were placed. It is important to try to keep the material density high across the piece of tape. Then in the glove box some squares of new Polydimethylsiloxane (PDMS) are cut and placed on the tape with the WTe_2 . They are pulled off the tape and then a SiO_2 chip is placed on the PDMS to put some flakes onto the SiO_2 chip. Once the PDMS has been removed from the chip they are searched to see if there are any flakes that have the right properties to be used in a stack. The WTe_2 flakes that are used for the stack are about 20-30 nm thick (under 100x they usually appear blue/turquoise) and it is important that there is a clear a-axis, which is the axis with broken symmetry.

The WTe_2 flakes tend to cleave along the a-axis with two parallel lines, and this is how we estimate the crystallographic orientation of the WTe_2 flakes we pick. Once WTe_2 is found the same process is done on hBN (hexagonal boron nitride), which does not need to be exfoliated in the argon environment. The process of exfoliation is nearly identical to that of WTe_2 except that no PDMS is used. hBN is extremely delicate and so it must be very carefully exfoliated. For this stack it is important that the hBN flake can fully cover the WTe_2 flake that was previously found.

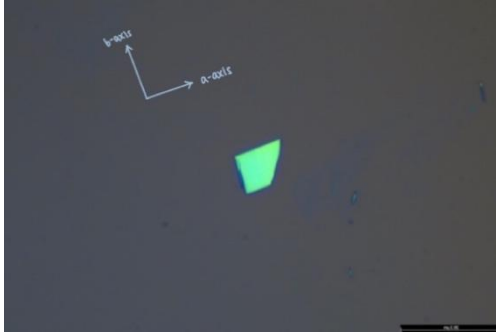


Figure 1 WTe₂ flake



Figure 2 hBN flake

The next step is stacking the flakes that were found. First a transfer slide of a thin film of Poly Bisphenol a Carbonate (PC) and PDMS is prepared by dropping PC solution onto one slide and using another slide to create an even layer of PC on the slide. PC is a thin film that is used to pick up the flakes. Using a razor and scotch tape a clean square of PC is isolated. On a larger slide a piece of PDMS (in a square) is placed at the center ensuring that the PDMS is completely touching the slide. Then the square of the PC is slowly draped onto the PDMS trying to have as few bubbles and wrinkles as possible. This is the slide that will be used to pick up the flakes that are going to be used in the stack. The microscope images of the flakes are used to plan the proposed stack. First the hBN flake is picked up with the transfer slide. A clean corner of the PDMS is pressed down on the chip with the hBN flake, close to the flake but not exactly on it. Then the stage is heated up to 85 degrees Celsius. Once the PC has crossed the flake the transfer slide is lifted off the chip and the flake are picked up by the PC film. Next the WTe₂ flake is located on the chip, and the hBN is located on the PC. The two flakes are then aligned using the optical microscope. This involves moving the PC slide till it is touching the chip a small amount and then focusing between the WTe₂ and the hBN to see how far off the alignment is. Once the alignment is completed the PC is pressed onto the chip and heated to 90 degrees Celsius to pick up WTe₂. Then the WTe₂ and hBN are put on the chip with pre-written marks for E beam lithography (EBL). The transfer slide is ripped off the slide and the hBN is left on the slide. Finally, the chip is cleaned off by melting PC in chloroform.



Figure 3 Stack before etching

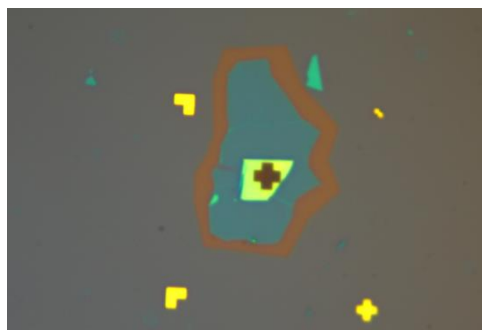


Figure 4 Stack after etching before iron milling

Once the chip is cleaned and checked under a microscope it is prepared for etching. The first step is to spin coat bilayer PMMA on the chip. The chips are spun at 3000 rpm so the resist will spread out uniformly onto the chip making a thin layer over the whole chip. After spin coating, the chip is baked at 170 C for 2 min to harden the resist. The E beam lithography is used to define the etch pattern to selectively deposit metal on or selectively etch a certain region. The hBN is etched into a Hall cross geometry by reactive ion etching.

Once this is complete the hBN is etched everywhere except on the cross. Ion milling is used afterward to remove excessive WTe₂ and the hBN acts as a mask to protect the remaining WTe₂. Ion milling is a more

aggressive sputtering as the acceleration voltage is much higher than for argon sputtering. The advantage is that argon is going in a straight line, so it is a clear line and it is a method of physical etching since there is no chemical reaction happening. The ion milling will also be used to etch TmIG to define the geometry of the devices.

After the whole stack is patterned into a Hall cross, a second EBL with MMA/ PMMA bilayer spin coat is performed to define the electrodes. The electrodes are made by depositing Ti (1nm) / Pt (6 nm)/ Au (70 nm) using e-beam evaporator in high vacuum with pressure in low e-7 Torr range. Pt is the main contact as the work function matches that of WTe₂. The excess of metal and the resist will be lifted off from the chip by immersing the chip in 55 C hot acetone. A pipette is then used to blow the acetone toward the chip to remove the resist and extra material from the chip. Once this is done the device is checked under a microscope before it is mounted.

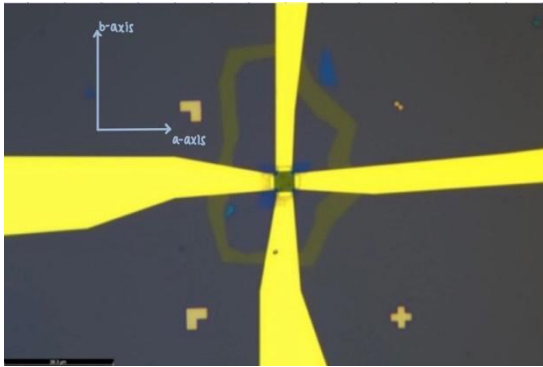


Figure 5 Device after iron milling and electrode deposition

The mounting process begins with shaping the chip carrier that is put into the experiment, the edges of the chip carrier are filed down and the top insulating coating that is on the electrodes is sanded down to expose the copper electrodes. Then the chip carrier is sonicated in IPA for 5 minutes. The device is then attached to the chip carrier using silver paste. This is left to dry and then the device is wire bonded to the electrodes on the chip carrier making a note of which electrodes are wire bonded. The carrier is then mounted onto the experimental device. Once there the electrodes are tested to make sure that the electric contact is present. After this is established the measurement can start.

To tell if the side contact was successful, we need to consider the resistance of the side contact device. First, we will measure the resistance of the device. By comparing the temperature dependence of the resistance to the previous WTe₂ devices, we can confirm if the side contact is good and if the properties of WTe₂ is not changed.

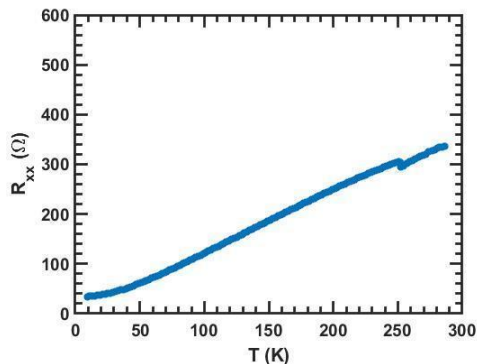


Figure 6 Resistance vs. Temperature for b-axis

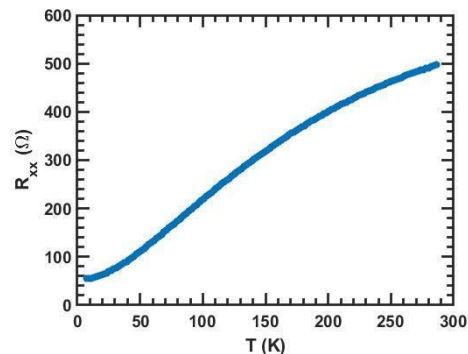


Figure 7 Resistance vs. Temperature for a-axis

These plots agree with what has been observed in previous experiments, so we know that this test worked. Thus, we continue on to making $WTe_2/TmIG$ stacks. Once the side contact device has been tested the next step is the actual $WTe_2/TmIG$ device. Many of the steps to making this device are the same as for the side contact device but they will be briefly outlined.

$WTe_2/TmIG$ devices:

First it is important to note that instead of stacking onto a SiO_2 chip everything will be stacked onto the TmIG sample provided to us by collaborators at CEM. The WTe_2 flakes that are used for the TmIG/ WTe_2 stacks are thin, about 1-5 nm thick (under 100x they usually appear dark blue) and it is important that there is a clear a-axis, which is the axis with broken symmetry. The WTe_2 flakes are exfoliated using the same method as outlined previously. The hBN provides a cap for the air sensitive WTe_2 . In the stacking process first the hBN is picked up, then the WTe_2 is picked up and aligned. Finally, the hBN and the WTe_2 are put down on the TmIG substrate surface.

Since for the side contact devices the WTe_2 will be etched it is extremely important to know what the a-axis is as the experiment relies on the broken in plane symmetry of WTe_2 . This can be determined using Polarized Raman Spectroscopy. Polarized Raman Spectroscopy involves looking at the discrete energy peaks of phonons in the material. This will make sure that the a-axis is the axis that we thought it was. There are two devices that were made to be sent to Polarized Raman Spectroscopy. The final stack images appear much darker than the stacks from the side contact device since here we are stacking onto the TmIG grown on SGGG. Below is a schematic side view of what a $WTe_2/TmIG$ stack would look like before it becomes a device. The WTe_2 is stacked on the TmIG and then is capped with hBN, the same method as the side contact device stack.



Figure 8 Side view of $WTe_2/TmIG$ stack

The flakes and the complete stack for the three devices are shown below. The third stack of $WTe_2/TmIG$, device 3, is the one that we made into a full device and will start doing measurements on. Below are the initial flakes that were used in the stack and the completed stack. The stacks appear to be almost transparent because they are being stacked onto the TmIG and SGGG substrate instead of the usual SiO_2 chips.



Figure 9 WTe_2 flake device 1

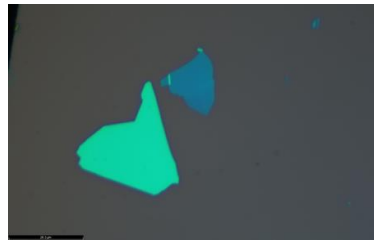


Figure 10 hBN flake device 1

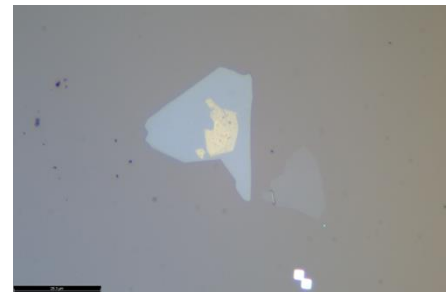


Figure 11 complete stack device 1

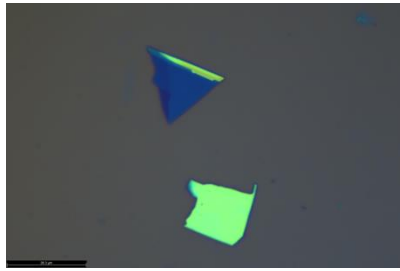


Figure 12 WTe₂ flake device 2

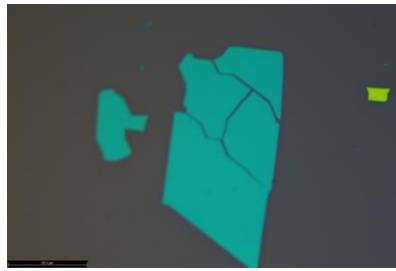


Figure 13 hBN flake device 2

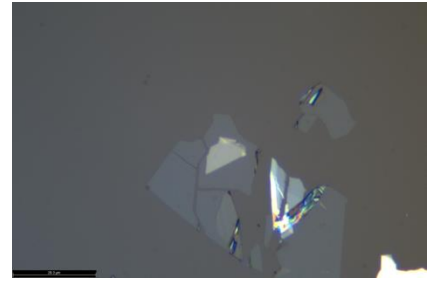


Figure 14 complete stack device 2

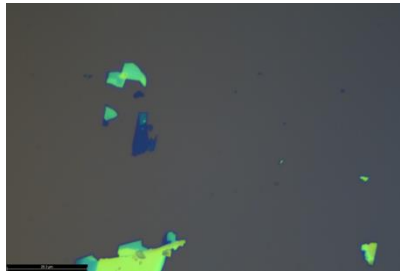


Figure 15 WTe₂ flake device 3

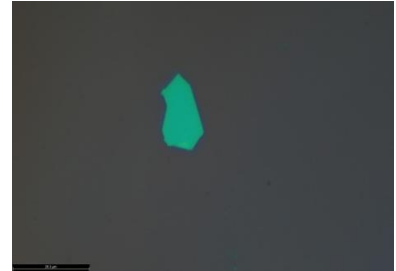


Figure 16 hBN flake for device 3



Figure 17 complete stack device 3

Once the stack is complete the process of making the stack into a device starts. First Atomic Force Microscopy (AFM) is performed on the complete stack to determine the thickness of the hBN and WTe₂ flakes. For AFM we use tapping mode to get a scan of the area and then using this scan gwyddion we can extract height information about the sample. This information is important for knowing how long the materials should be etched for. Below are pictures of the AFM scans and the corresponding analysis graphs that show the height differences.

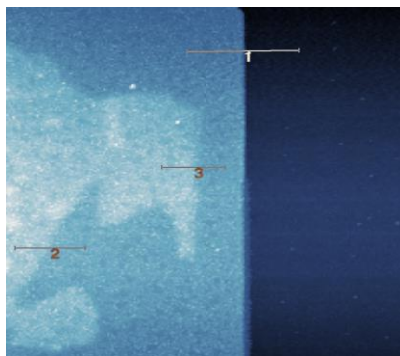


Figure 18 AFM scan

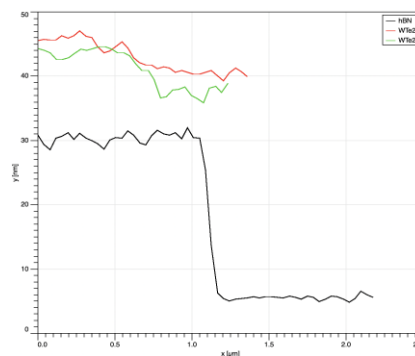


Figure 19 Height difference graph from AFM scan gwyddion

From the AFM data we know that the hBN is about ~25 nm thick and the WTe₂ is about 5nm thick which is consistent with the color that we were of the flakes. The next step is taking the stack and making it into a device. The schematic side views of this are shown below. First the whole stack is spin coated in PMMA.



Figure 20 Side view of first spin coated stack

Then using E-beam lithography a pattern designed using CAD is created. After this step, the hBN is etched using Reactive Ion Etching (RIE) using CHF₃/CF₄ gas. Then the PMMA is removed by putting the chip into PG remover at 65 deg C for 20 mins and then in 55 deg C acetone for 20 mins then rinsed with IPA and blow dried.



Figure 21 Side view of after RIE etching to remove hBN

Once the hBN has been removed WTe₂ and TmIG have to be etched using Ion Milling. Below is a graph (Figure 23) from the etch process. The blue line is Iron, and the black line is Thulium. From this graph we can see as indicated by the green star that at 10 secs we start to etch the TmIG and the iron signal increased. After about 6 seconds it goes back to background level and then the sample is etched for 10 more secs to account for the etch time of WTe₂.



Figure 22 Side view after iron milling away TmIG and WTe₂

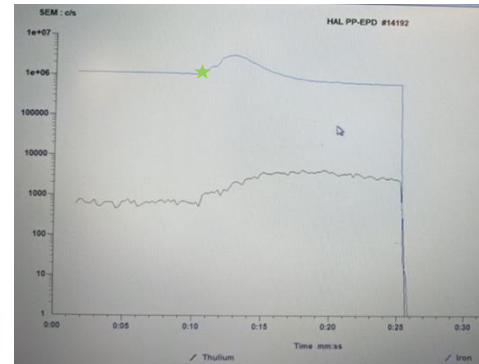


Figure 23 Etch rates

The next step is to add to the electrodes. First the stack is spin coated again. Then using E-beam lithography the electrodes are patterned. Once this is done it is Argon sputtered and then Ti/Pt is deposited everywhere on the chip. Finally, the excess metal is lifted off using hot acetone. Then the device is complete.



Figure 24 Side view of electrodes and TmIG/ WTe₂ complete device

Below is an image of the stack after this ion milling etching as well as an image of the complete device with electrodes. The green outline is where the hBN flake was and the yellow outline is where the WTe₂ flake was. In the middle there is the 8-pin design that will be attached to the electrodes. We chose to do 8 pins so that we could send current in 3 different directions since the physics is different along different crystal axis in WTe₂.



Figure 25 Stack after etching

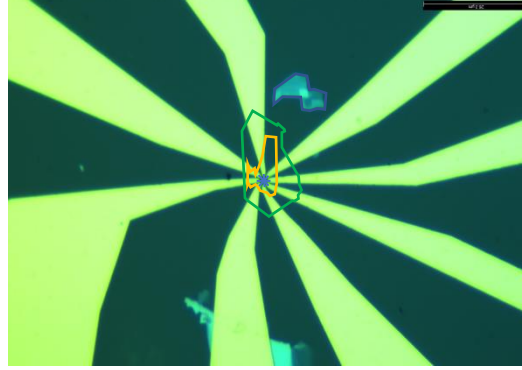


Figure 26 Complete device with electrodes

III. Results and Discussion

Once the device is complete it will be measured. In the mounting process the electrodes will be wire bonded to the chip carrier for electric contacts in the experiment. The cryostat can go to 7 K and a magnetic field of up to 1.2 T can be applied and the magnet can be rotated. Once the device is mounted, the first test is for electric contact, to ensure that all of the electrodes are working, and electric contact is made. The next measurements are of the Hall resistance. With this measurement we are looking for a hysteresis loop which will be due to TmIG since it is magnetic unlike WTe_2 . If we see the hysteresis loop, we will try to observe switching in the device as demonstrated in the previous experiment.

IV. Conclusions

We have found a way to make side contact devices for materials that are grown on substrates. In addition, we have made a device of WTe_2/TmIG that can be measured to look for spin orbit torque deterministic switching.

V. Acknowledgements

Thanks to Professor Katoch and Professor Singh for providing me with this opportunity. Thanks to I-Hsuan Kao for helping me with this project. This research was primarily supported by the Center for Emergent Materials, an NSF MRSEC, under award number DMR-2011876.

VI. Footnotes, Endnotes and References

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